

Figure 1
programmable
logic device 10

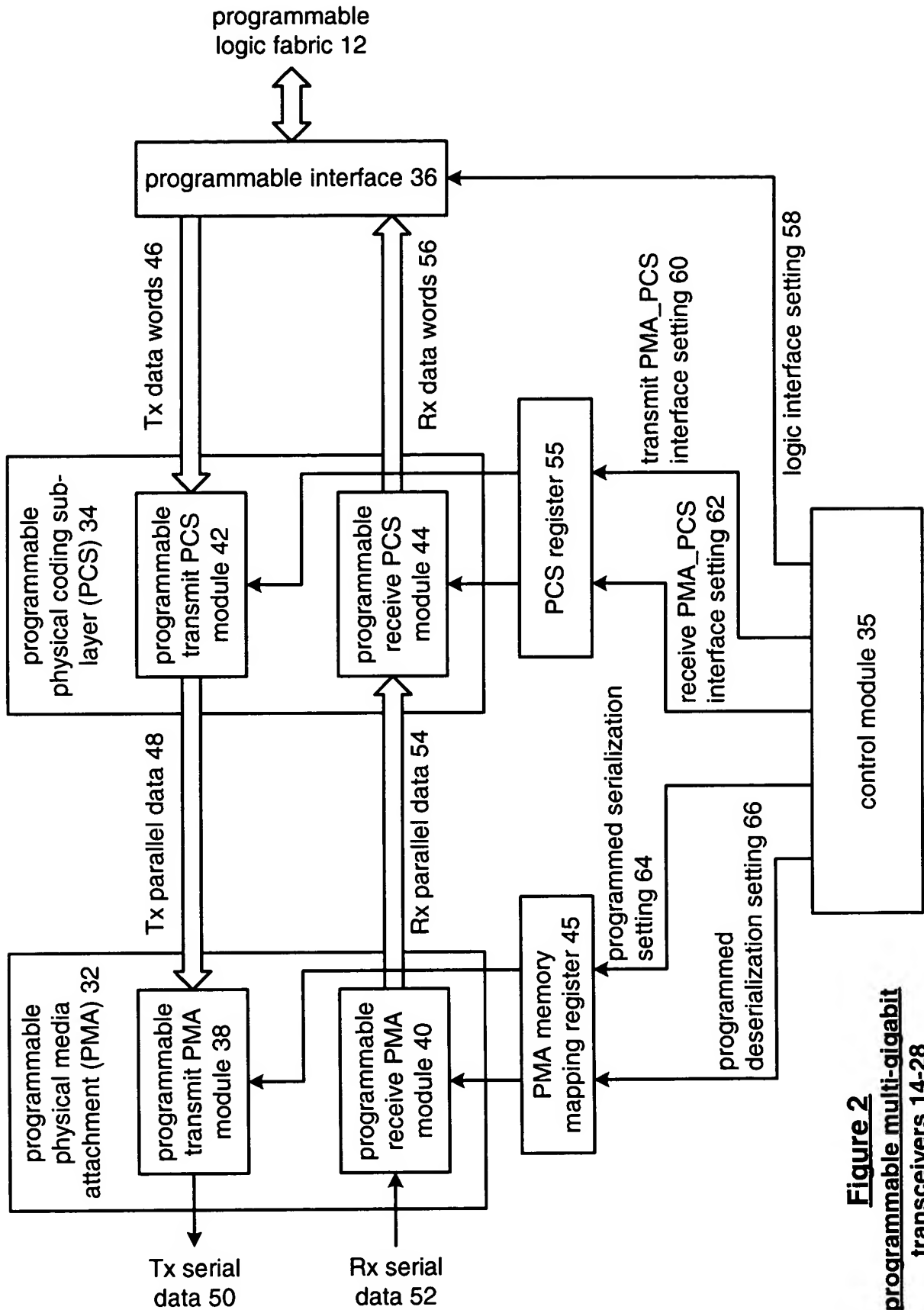


Figure 2
programmable multi-gigabit
transceivers 14-28

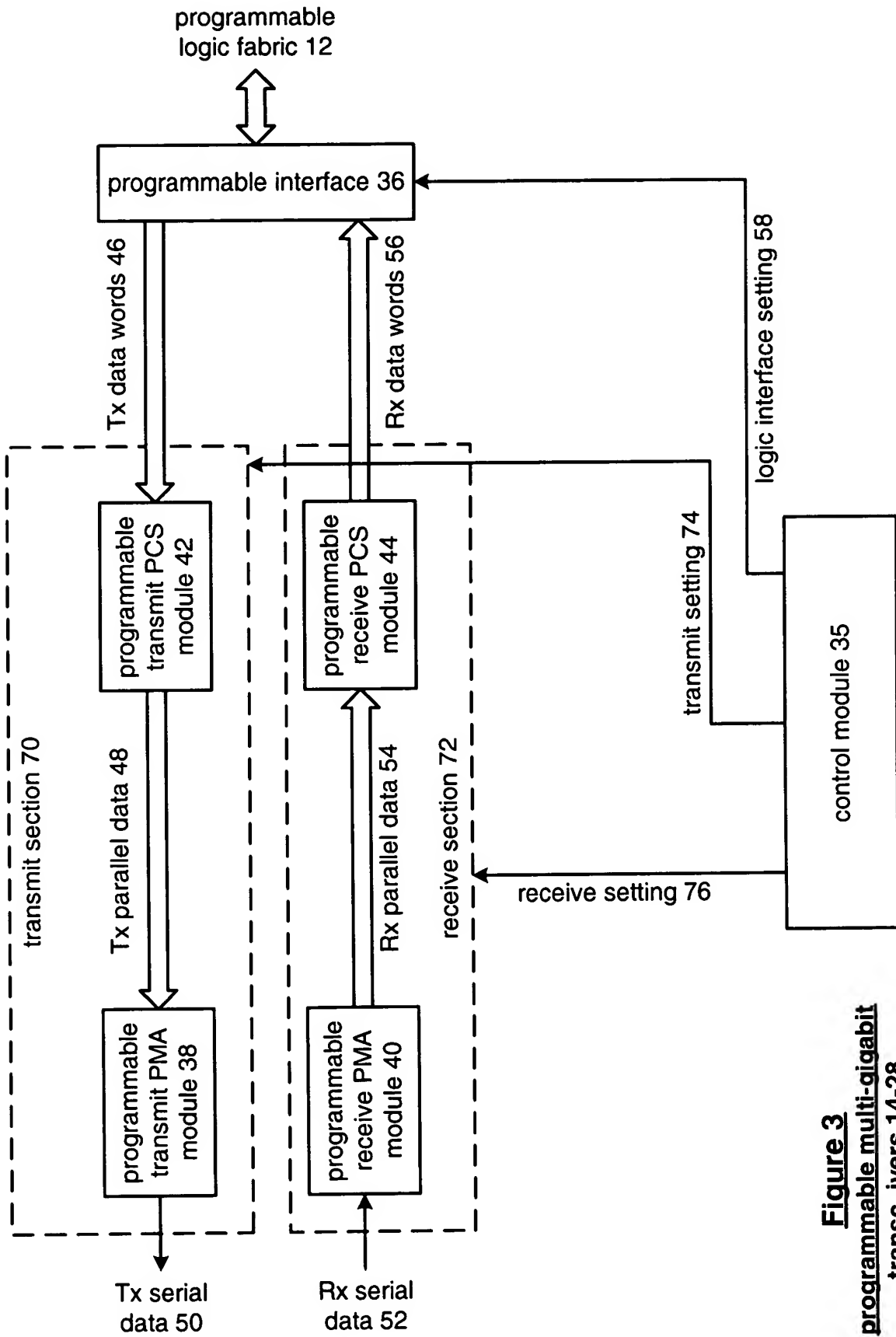


Figure 3
programmable multi-gigabit
transceivers 14-28

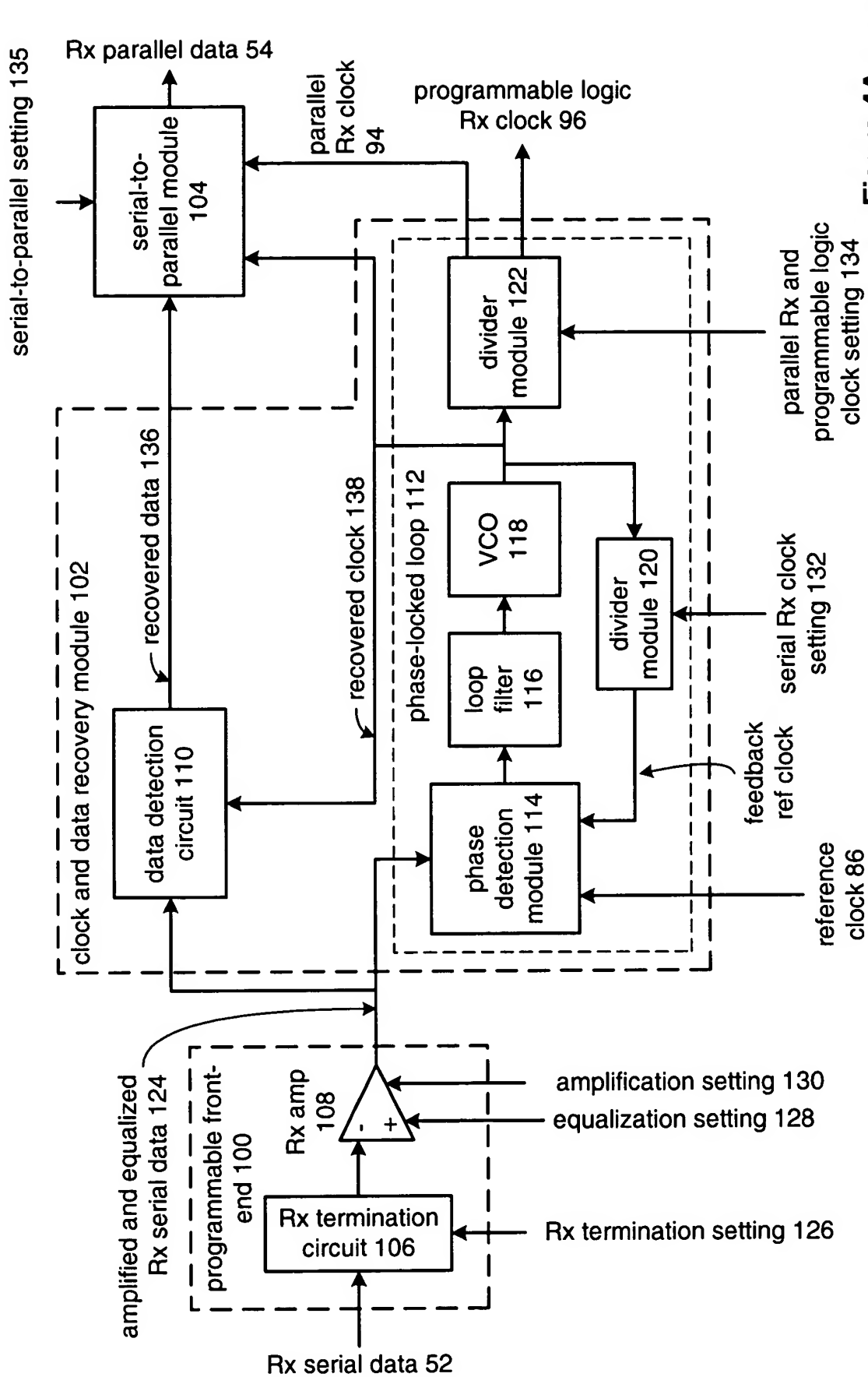


Figure 4A
 programmable r ceiv
 PMA module 40

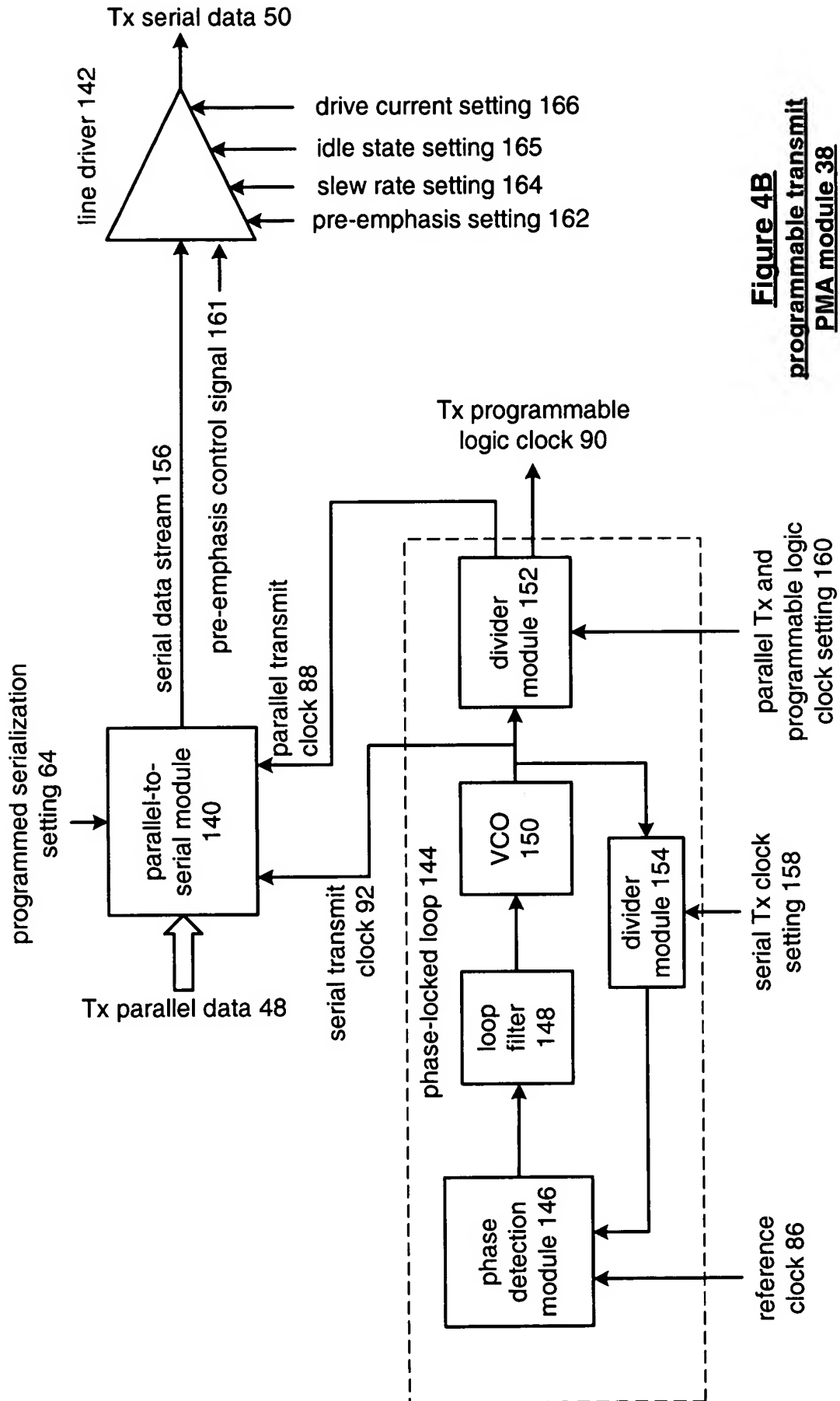


Figure 4B
programmable transmit
PMA module 38

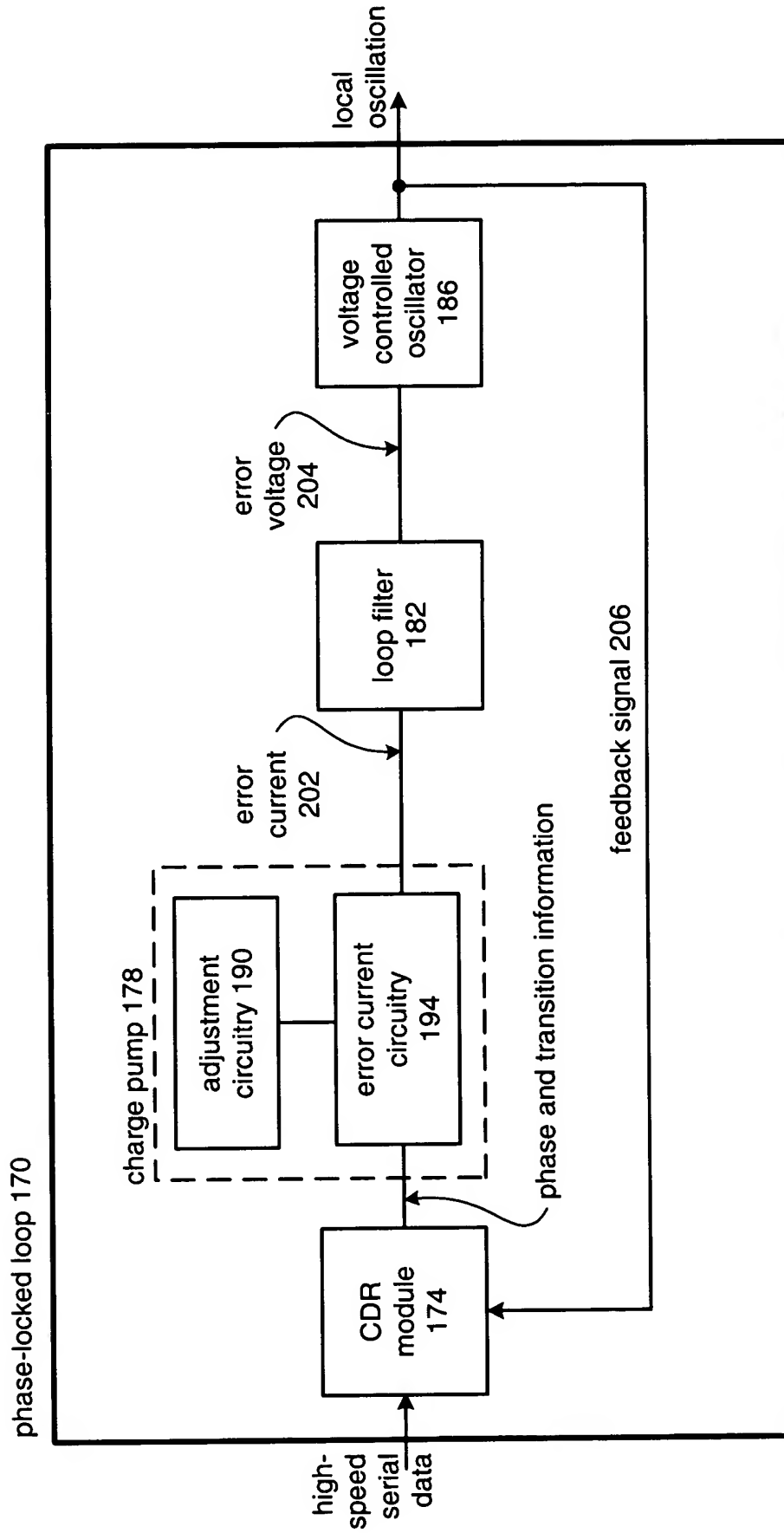


Figure 5
phase-locked loop 170

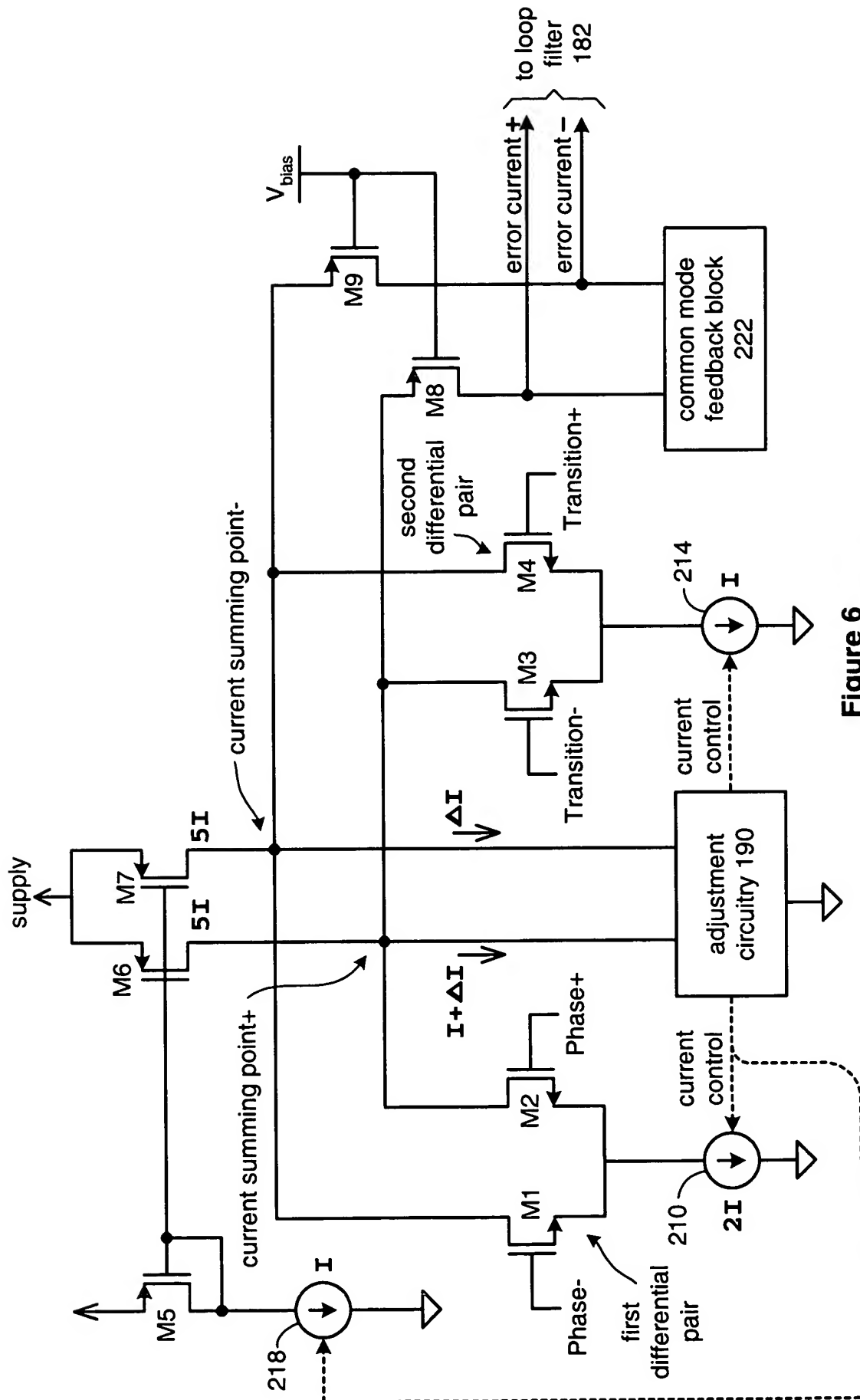


Figure 6
charge pump 178

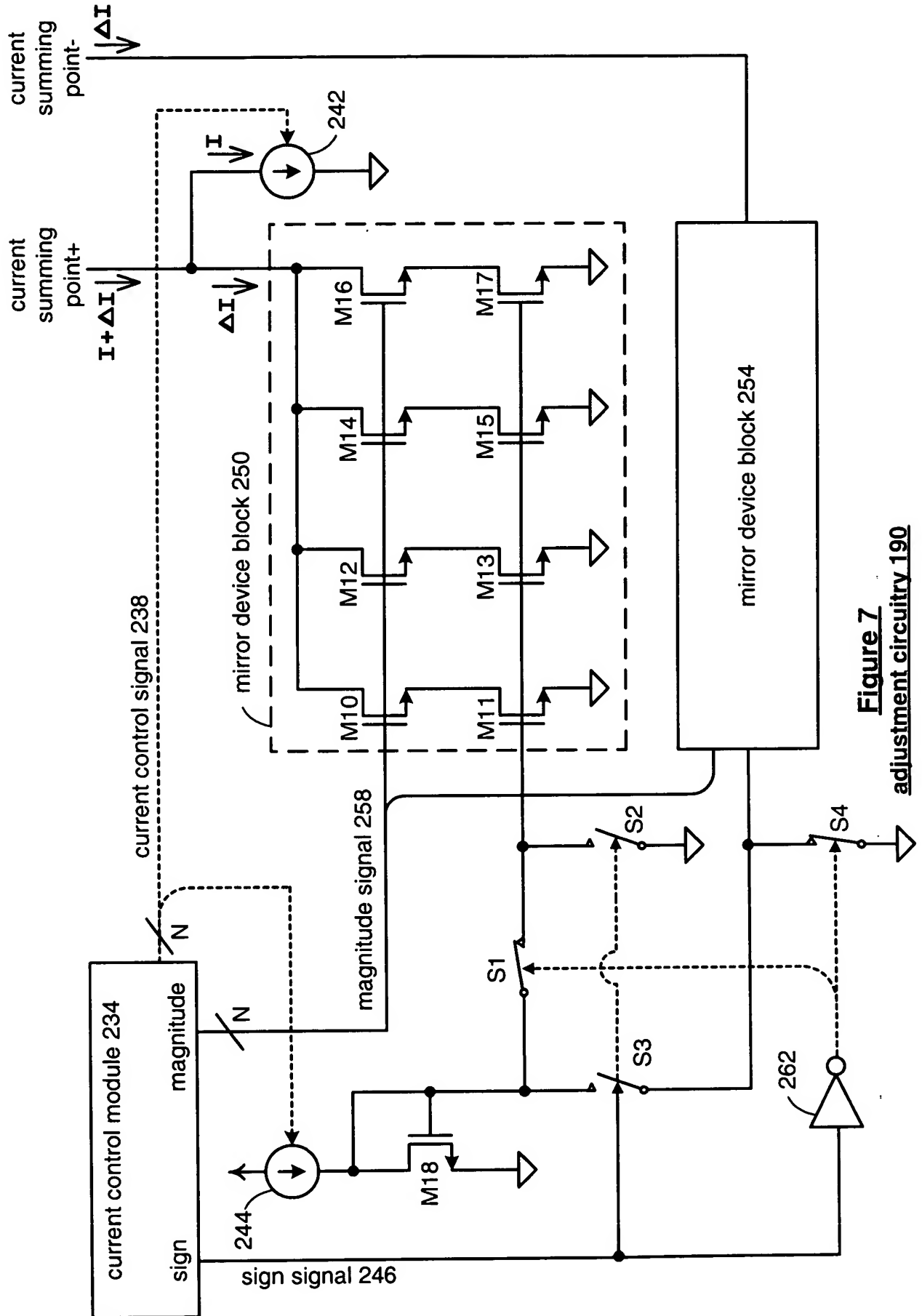


Figure 7
adjustment circuitry 190

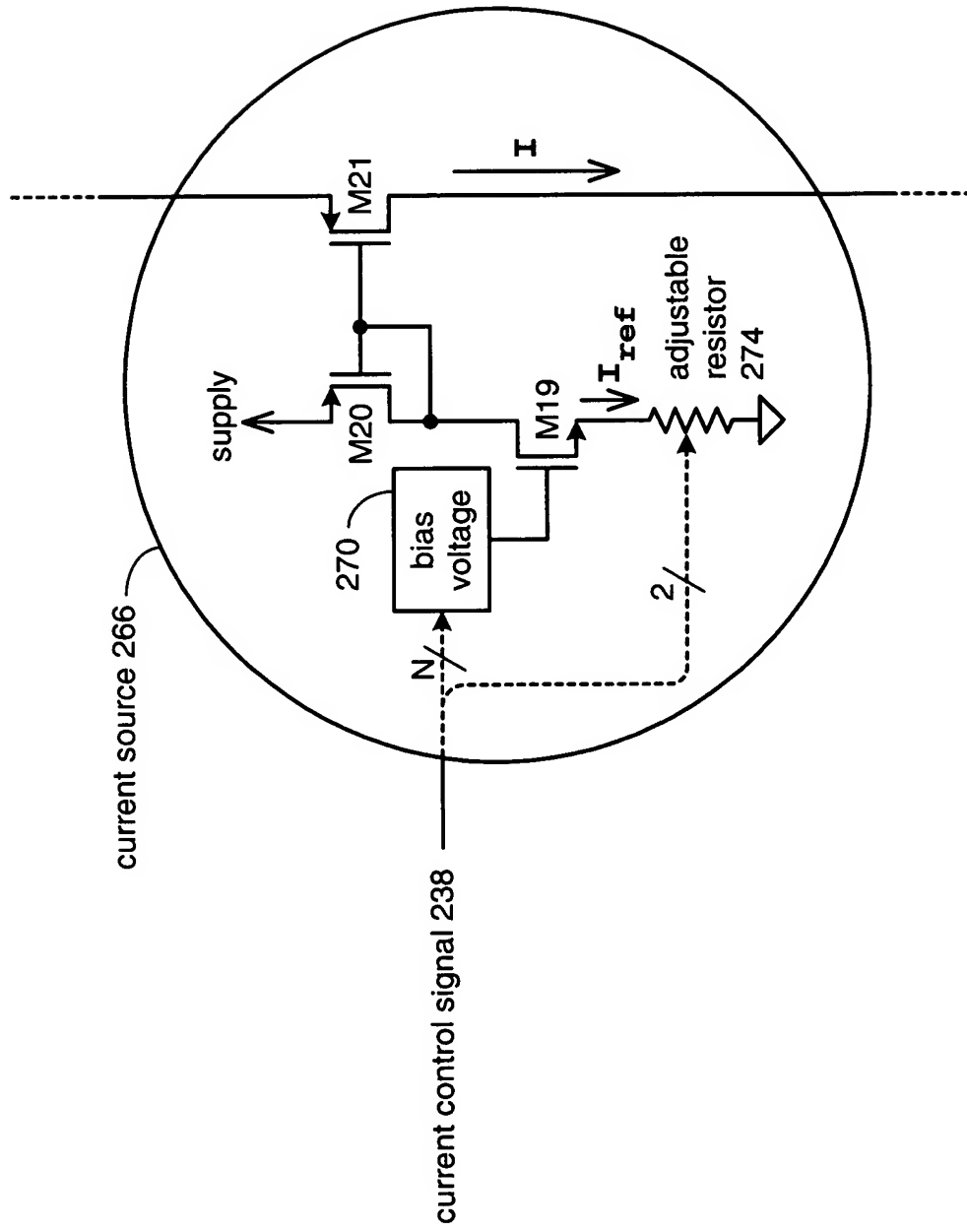


Figure 8
adjustable current source

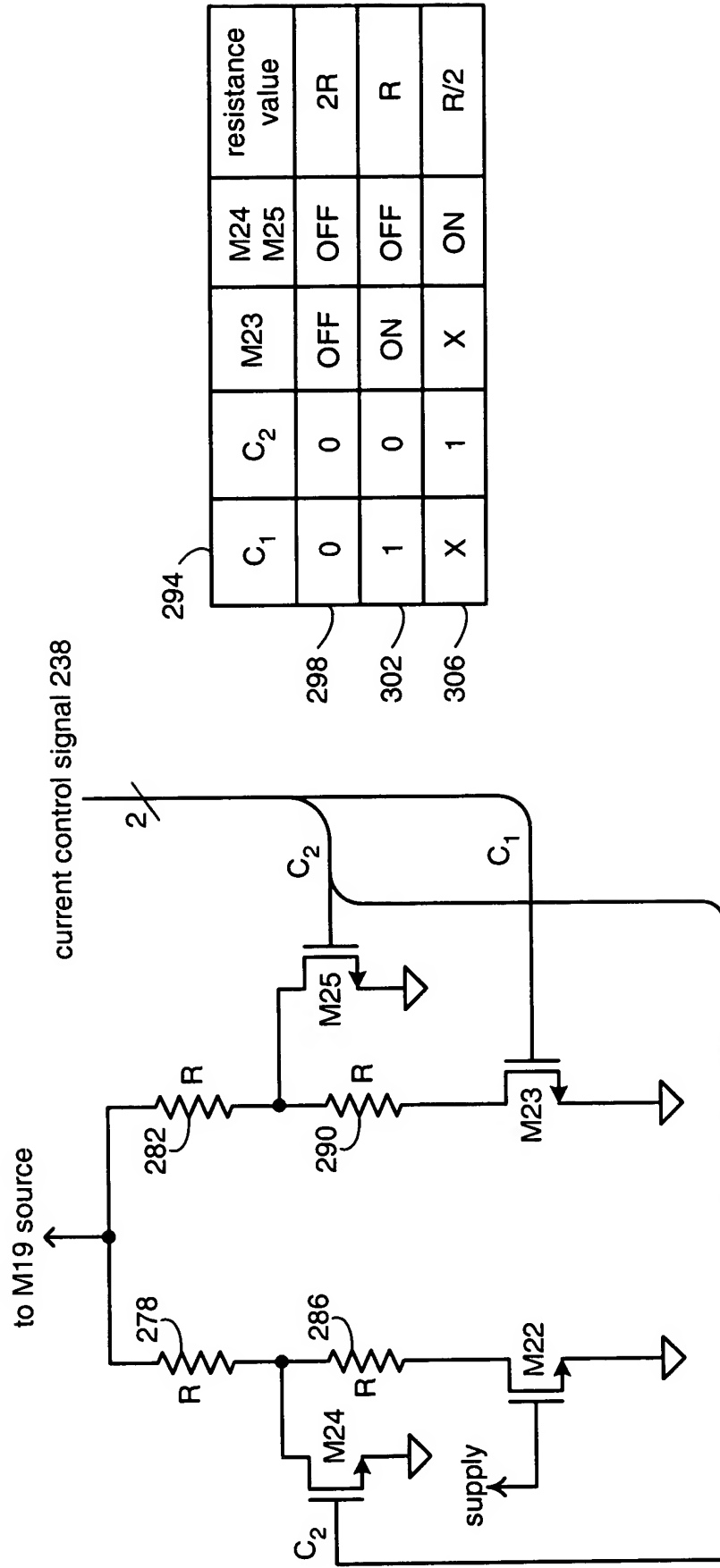


Figure 9
adjustable resistor 274

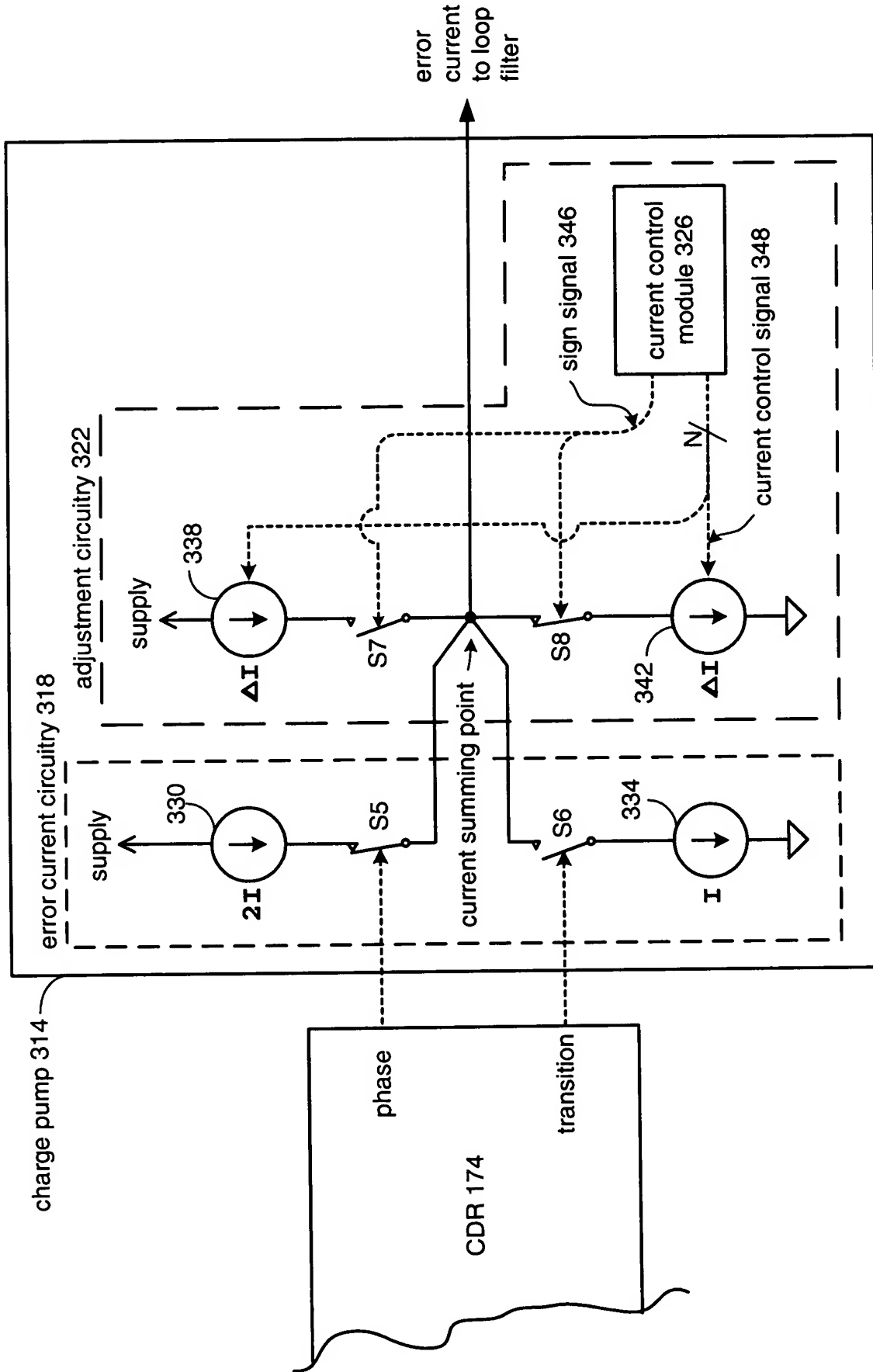


Figure 10
charge pump alternate embodiment

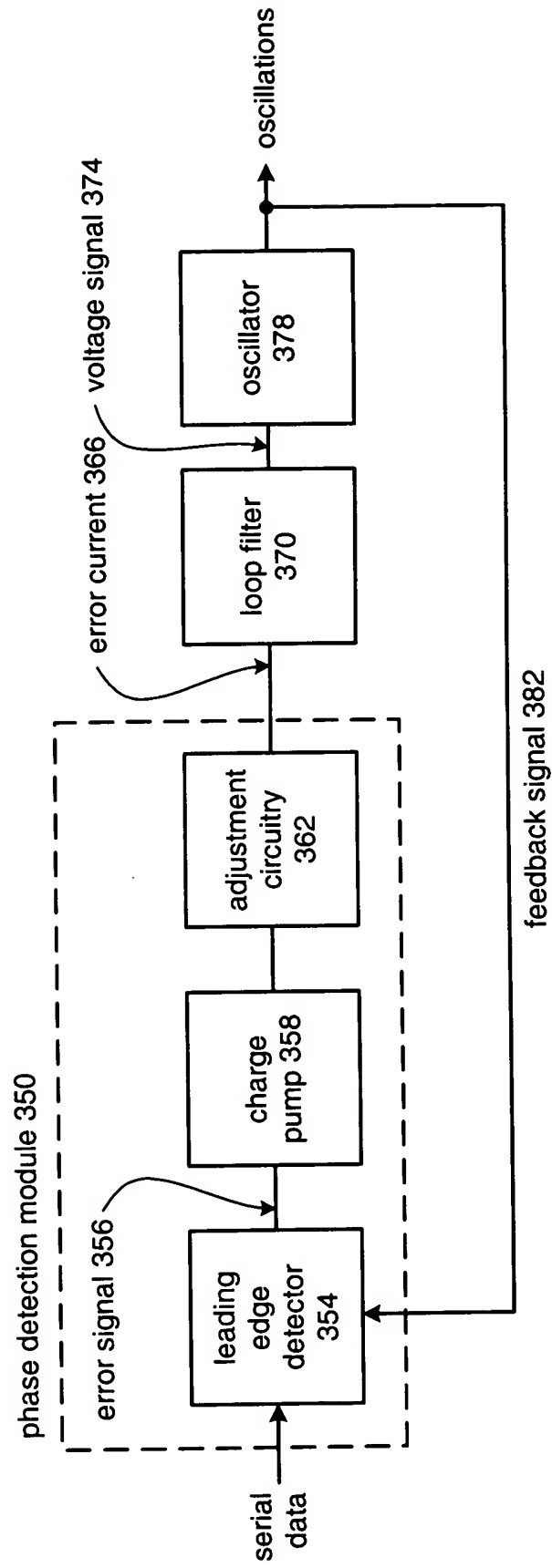


Figure 11
phase detection module

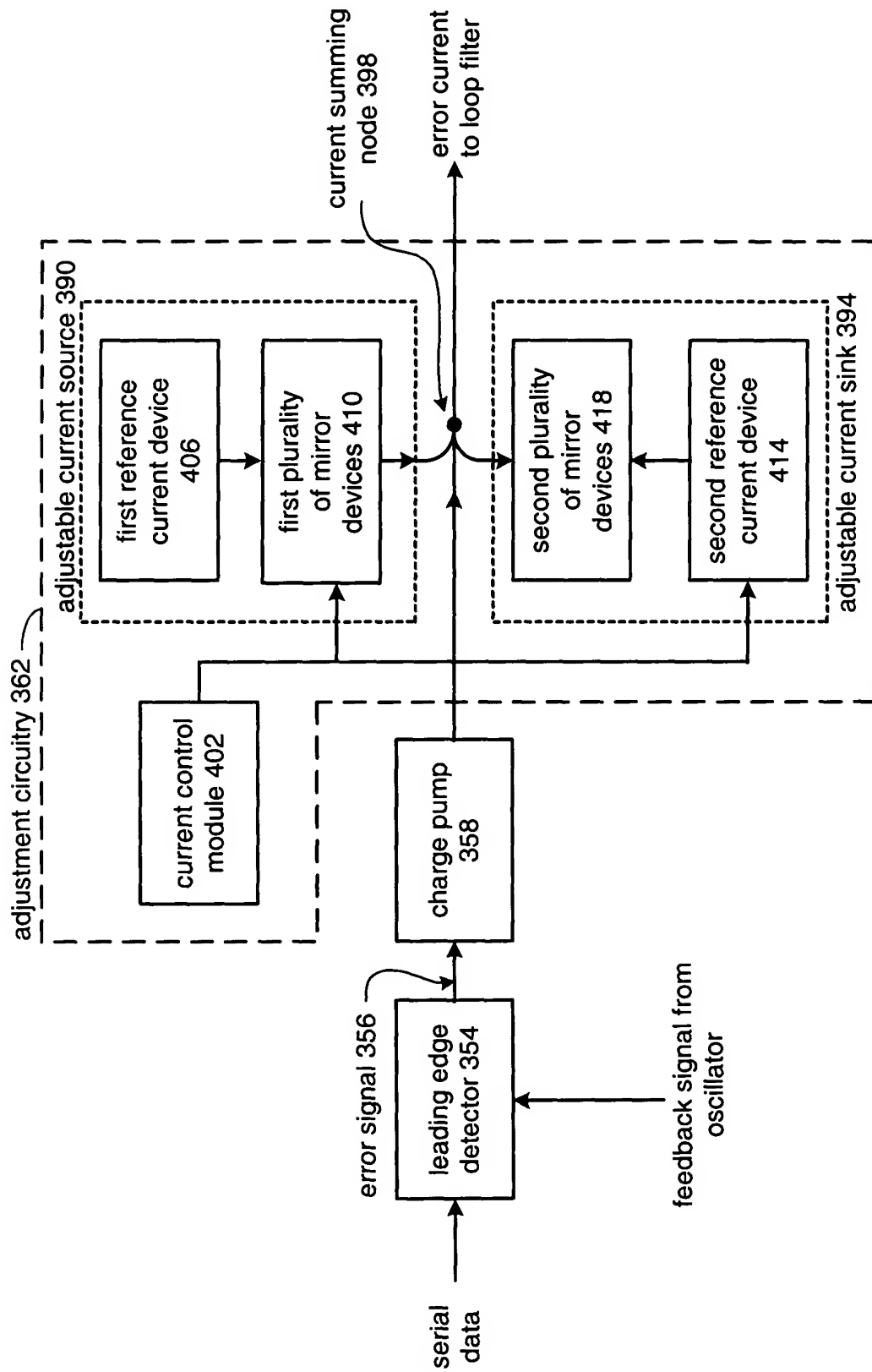


Figure 12
phase detector section 350

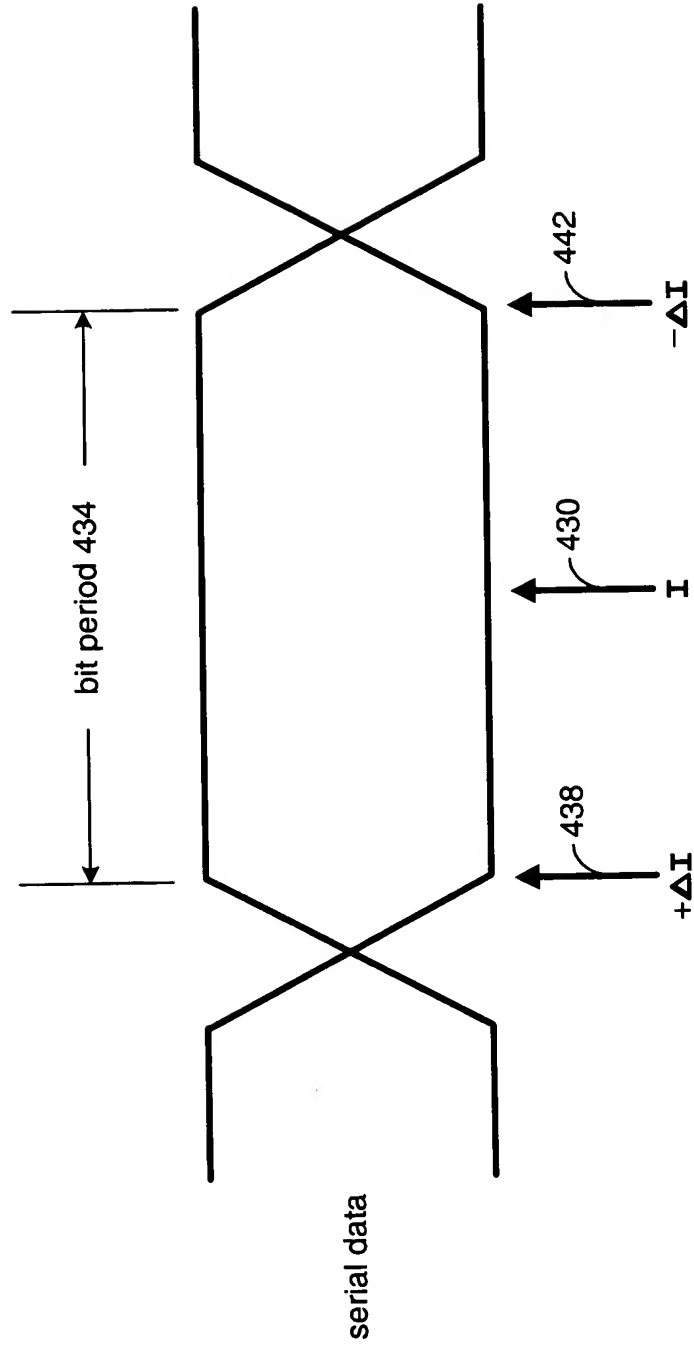


Figure 13
serial data y diagram

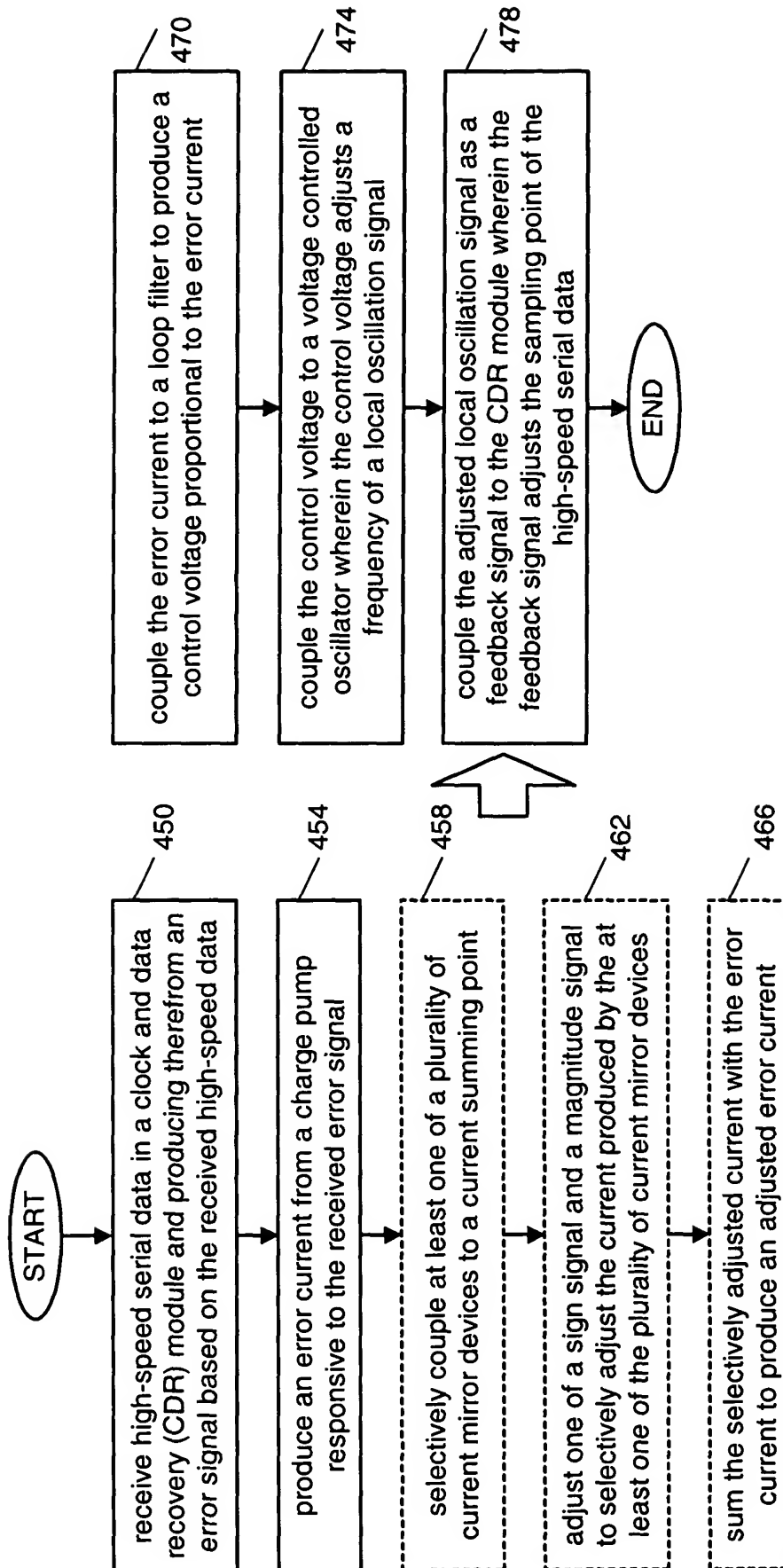


Figure 14
PLL sampling point adjustment method